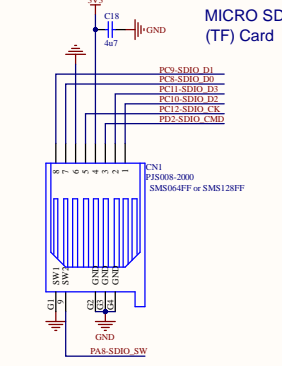
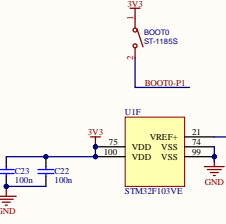
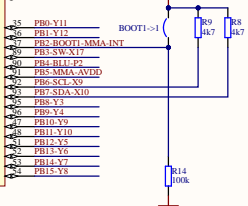


U1E	PE2/TRACECLK / FSMC_A23 / ETH_MII_TXD3 / EVENTOUT	1	PE3
	PE3/TRACECLK / FSMC_A19 / EVENTOUT	2 <td>PE4</td>	PE4
	PE4/TRACECLK / FSMC_A20 / DCM1_D4 / EVENTOUT	3 <td>PE5</td>	PE5
	PE5/TRACECLK / FSMC_A21 / TM9_CH1 / DCM1_D6 / EVENTOUT	4 <td>PE6</td>	PE6
	PE6/TRACECLK / FSMC_A22 / TM9_CH2 / DCM1_D7 / EVENTOUT	5 <td>PE7</td>	PE7
	PE7/FSMC_D4/TM1_ETR / EVENTOUT	38 <td>PE8</td>	PE8
	PE8/FSMC_D5 / TM1_CH1N / EVENTOUT	40 <td>PE9</td>	PE9
	PE9/FSMC_D6/TM1_CH1 / EVENTOUT	41 <td>PE10</td>	PE10
	PE10/FSMC_D7/TM1_CH2N / EVENTOUT	42 <td>PE11</td>	PE11
	PE11/FSMC_D8/TM1_CH2 / EVENTOUT	43 <td>PE12</td>	PE12
	PE12/FSMC_D9/TM1_CH3N / EVENTOUT	44 <td>PE13</td>	PE13
	PE13/FSMC_D10/TM1_CH3 / EVENTOUT	45 <td>PE14</td>	PE14
	PE14/FSMC_D11/TM1_CH4 / EVENTOUT	46 <td>PE15</td>	PE15
	PE15/FSMC_D12/TM1_BK1N / EVENTOUT	46 <td>PE15</td>	PE15
<b>PD8/FSMC_D13 / USART1_TX / EVENTOUT</b>			
<b>PD9/FSMC_D14 / USART1_RX / EVENTOUT</b>			
<b>PD10/FSMC_D15 / USART1_CK / EVENTOUT</b>			
<b>PD11/FSMC_CLE / FSMC_A16/USART1_CTS / EVENTOUT</b>			
<b>PD12/FSMC_ALE / FSMC_A17/TM4_CH1 / USART1_RTS / EVENTOUT</b>			
<b>PD13/FSMC_A18/TM4_CH2 / EVENTOUT</b>			
<b>PD14/FSMC_D0/TM4_CH3 / EVENTOUT</b>			
<b>PD5/FSMC_D1/TM4_CH4 / EVENTOUT</b>			
<b>PD0/FSMC_D2/CAN1_RX / EVENTOUT</b>			
<b>PD1/FSMC_D3/CAN1_TX / EVENTOUT</b>			
<b>PD8/FSMC_CLE / USART2_CTS / EVENTOUT</b>			
<b>PD4/FSMC_NOE / USART2_RTS / EVENTOUT</b>			
<b>PD5/FSMC_NWE/USART2_TX / EVENTOUT</b>			
<b>PD6/FSMC_NWAIT / USART2_RX / EVENTOUT</b>			
<b>PD7/USART2_CK/FSMC_NE1 / FSMC_NC2 / EVENTOUT</b>			
<b>PD8/TM4_ETR / FSMC_NBE1 / DCM1_D2 / EVENTOUT</b>			
<b>PE1/FSMC_NBE1 / DCM1_D3 / EVENTOUT</b>			

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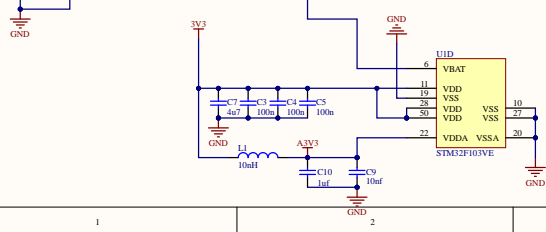
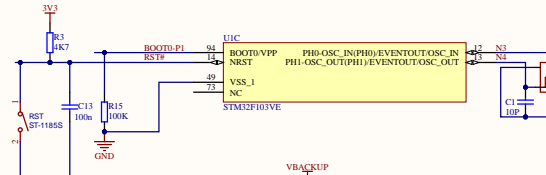


U1A	PA0/WKUP/PA0/USART_CTS/USART1_TX/ETH_MII_CRS/TM2_CH1_ETR/TM5_CH1/TM1_ETR/EVENTOUT/ADC12_IN0/WKUP	43	PA0_X1
	PA1/USART2_RTS/ART4_RX/ETH_RMII_RX_CLK/ETH_MII_RX_CLK/TM5_CH2/TM1_CH2/EVENTOUT/ADC12_IN1 <td>44 <th>PA1_X2</th> </td>	44 <th>PA1_X2</th>	PA1_X2
	PA2/USART2_TX/TM5_CH3/TM9_CH1/TM2_CH1/TM2_CH3/ETH_MDIO/EVENTOUT/ADC12_IN2 <td>45 <th>PA2_X3</th> </td>	45 <th>PA2_X3</th>	PA2_X3
	PA3/USART2_RX/TM5_CH4/TM9_CH2/TM2_CH2/OTG_HS_ULPI_D0/ETH_MII_CRS/EVENTOUT/ADC12_IN3 <td>46 <th>PA3_X4</th> </td>	46 <th>PA3_X4</th>	PA3_X4
	PA4/SPI1_NSS/SPI3_NSS/USART2_CK/DCM1_HS/NC/OTG_HS_SF/12S3_WS/EVENTOUT/ADC12_IN4/DAC_OUT1 <td>47 <th>PA4_X5</th> </td>	47 <th>PA4_X5</th>	PA4_X5
	PA5/SPI1_SCK/OTG_HS_ULPI_CK/TM2_CH1_ETR/TM5_CH1N/EVENTOUT/ADC12_IN5/DAC_OUT2 <td>48 <th>PA5_X6</th> </td>	48 <th>PA5_X6</th>	PA5_X6
	PA6/SPI1_MISO/TM8_BRN/TM3_CH1/TM1_BK1N/EVENTOUT/ADC12_IN6 <td>49 <th>PA6_X7</th> </td>	49 <th>PA6_X7</th>	PA6_X7
	PA7/SPI1_MOSI/TM8_CH1N/TM4_CH1/TM3_CH2/ETH_MII_RX_DV/TM1_CH1N/ETH_RMII_CRS_DV/EVENTOUT/ADC12_IN7 <td>50 <th>PA7_X8</th> </td>	50 <th>PA7_X8</th>	PA7_X8
	PA8/MCO/USART1_CK/TM1_CH1C23_SCL/OTG_HS_SF/EVENTOUT <td>51 <th>PA8_X9</th> </td>	51 <th>PA8_X9</th>	PA8_X9
	PA9/USART1_TX/TM1_CH2/12C3_SMB/A/DCM1_D0/EVENTOUT/OTG_FS_VBUS <td>52 <th>PA9/SDIO_SW</th> </td>	52 <th>PA9/SDIO_SW</th>	PA9/SDIO_SW
	PA10/USART1_RX/TM1_CH2/OTG_FS_ID/DCM1_D1/EVENTOUT <td>53 <th>PA10</th> </td>	53 <th>PA10</th>	PA10
	PA11/USART1_CTS/CAN1_RX/TM1_CH3/OTG_FS_DM/EVENTOUT <td>54 <th>PA11_DM</th> </td>	54 <th>PA11_DM</th>	PA11_DM
	PA12/USART1_RTS/CAN1_TX/TM1_ETR/OTG_FS_DP/EVENTOUT <td>55 <th>PA12_DP</th> </td>	55 <th>PA12_DP</th>	PA12_DP
	PA13/TM5_SWIO0/TM5_SWIO0/EVENTOUT <td>56 <th>PA13-RED-P5</th> </td>	56 <th>PA13-RED-P5</th>	PA13-RED-P5
	PA14/OTG_HS_VL1/PC13_SWCLK/OTG_FS_SWCLK/EVENTOUT <td>57 <th>PA14-GRN-P4</th> </td>	57 <th>PA14-GRN-P4</th>	PA14-GRN-P4
	PA15/SDIO_D1/SPI3_NSS/12S3_WS/TM2_CH1_ETR/SPI1_NSS/EVENTOUT <td>57 <th>PA15-YEL-P3</th> </td>	57 <th>PA15-YEL-P3</th>	PA15-YEL-P3

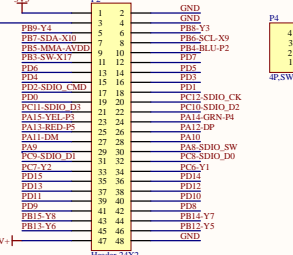
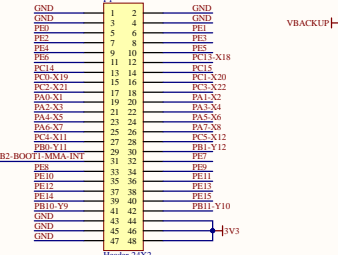


U1B	PC0/OTG_HS_ULPI_STP/EVENTOUT/ADC12_IN10	45	PC0_X19
	PC1/ETH_MD0/EVENTOUT/ADC12_IN11 <td>46 <th>PC1_X20</th> </td>	46 <th>PC1_X20</th>	PC1_X20
	PC2/SPI2_MISO/OTG_HS_ULPI_DIR/ETH_MII_TXD2/12S2a_SD/EVENTOUT/ADC12_IN12 <td>47 <th>PC2_X21</th> </td>	47 <th>PC2_X21</th>	PC2_X21
	PC3/SPI2_MOSI/12S2_SD/OTG_HS_ULPI_NST/ETH_MII_TX_CLK/EVENTOUT/ADC12_IN13 <td>48 <th>PC3_X22</th> </td>	48 <th>PC3_X22</th>	PC3_X22
	PC4/ETH_RMII_RX_D0/ETH_MII_RX_D0/EVENTOUT/ADC12_IN14 <td>49 <th>PC4_X23</th> </td>	49 <th>PC4_X23</th>	PC4_X23
	PC5/ETH_RMII_RX_D1/ETH_MII_RX_D1/EVENTOUT/ADC12_IN15 <td>50 <th>PC5_X24</th> </td>	50 <th>PC5_X24</th>	PC5_X24
	PC6/12S2_MCK/TM8_CH1/SDIO_D6/USART6_TX/DCM1_D0/TM1_CH1/EVENTOUT <td>51 <th>PC6-Y1</th> </td>	51 <th>PC6-Y1</th>	PC6-Y1
	PC7/12S3_MCK/TM8_CH2/SDIO_D7/USART6_RX/DCM1_D1/TM1_CH2/EVENTOUT <td>52 <th>PC7-Y2</th> </td>	52 <th>PC7-Y2</th>	PC7-Y2
	PC8/TM8_CH3/SDIO_D8/TM1_CH2/USART6_CK/DCM1_D2/EVENTOUT <td>53 <th>PC8-SDIO_D0</th> </td>	53 <th>PC8-SDIO_D0</th>	PC8-SDIO_D0
	PC9/12S3_CKIN/MCO2/TM8_CH4/SDIO_D9/12C3_SDA/DCM1_D3/TM1_CH3/EVENTOUT <td>54 <th>PC9-SDIO_D1</th> </td>	54 <th>PC9-SDIO_D1</th>	PC9-SDIO_D1
	PC10/SPI1_SCK/12S3_CK/ART4_TX/SDIO_D10/DCM1_D4/USART1_TX/EVENTOUT <td>55 <th>PC10-SDIO_D2</th> </td>	55 <th>PC10-SDIO_D2</th>	PC10-SDIO_D2
	PC11/ART4_RX/SPI1_MISO/SDIO_D11/DCM1_D4/USART1_RX/12S3a_SD/EVENTOUT <td>56 <th>PC11-SDIO_D3</th> </td>	56 <th>PC11-SDIO_D3</th>	PC11-SDIO_D3
	PC12/UART5_TX/SDIO_CK/DCM1_D9/SPI1_MOSI/12S3_SD/USART1_CK/EVENTOUT <td>57 <th>PC12-SDIO_CK</th> </td>	57 <th>PC12-SDIO_CK</th>	PC12-SDIO_CK
	PC13/EVENTOUT/RTC_OUT/RTC_SMP/RTC_FS <td>58 <th>PC13-X18</th> </td>	58 <th>PC13-X18</th>	PC13-X18
	PC14/ART4_RX/SPI1_MISO/SDIO_D12/DCM1_D4/USART1_RX/12S3a_SD/EVENTOUT <td>59 <th>PC14</th> </td>	59 <th>PC14</th>	PC14
	PC14-OSC2_IN/PC14/EVENTOUT/OSC2_IN <td>60 <th>PC14</th> </td>	60 <th>PC14</th>	PC14
	PC15-OSC3_OUT/PC15/EVENTOUT/OSC3_OUT <td>61 <th>PC15</th> </td>	61 <th>PC15</th>	PC15
<b>PD2/TM1_ETR/UART5_RX/SDIO_CMD/DCM1_D1/EVENTOUT</b>			

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VCC-GND.COM		
Title	Number	Revision
A2	7/12/2023	
Date:	7/12/2023	Sheet of
File:	E5023年硬件设计11-VD-Fyboard Sch	Drawn By: